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Digital signal acquisition system for complex nuclear reaction experiments

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Abstract
A digital data-acquisition system based on XIA LLC products was used in a complex nuclear reaction experiment using radioactive ion beams. A flexible trigger system based on a field-programmable gate array (FPGA) parametrization was developed to adapt to different experimental sizes. A user-friendly interface was implemented, which allows converting script language expressions into FPGA internal control parameters. The proposed digital system can be combined with a conventional analog data acquisition system to provide more flexibility. The performance of the combined system was verified using experimental data.

Keywords Digital signal acquisition system · Trigger · Programmable logic · Timestamp

1 Introduction

Currently, one of the frontiers of nuclear physics studies is the exploration of exotic structures in unstable nuclei [1–4]. Experiments on unstable nuclei are generally based on the availability of secondary radioactive ion beams, which generally suffer from low beam intensity. Accordingly, such experiments generally require more complicated detection systems, resulting in more electronic channels and complicated trigger systems [5–8].

Traditionally, analog data acquisition systems have been implemented based on several standards such as CAMAC and VME [9–11]. Conventionally, this system comprises several layers of electronic units, including a preamplifier, shaping amplifier, analog-to-digital converter (ADC) for the analog signal channel, fast amplifier, discriminator, and time-to-digital converter (TDC) for the timing signal. The ADC or TDC extracts (buffers) the energy (amplitude) or timing information under the control of the trigger system [11, 12]. The trigger is typically generated from the coincidence of selected fast signals corresponding to the physical process of interest.

In recent years, along with the progress in fast digitizing techniques, digital data acquisition (DDAQ) systems have been developed and widely adopted. In a DDAQ system, sampling and digitization are implemented directly on the signals from the preamplifier. The sampling frequency must be sufficiently high (generally higher than 100 MHz) to retain the original information transmitted by the analog signal [13–16]. The energy (amplitude) and time information of the preamplified signal can then be extracted using well-designed digital manipulation methods. In this manner, the hardware electronic layers between the preamplifier and digital system, such as the main amplifier, discriminator, ADC, and TDC, are replaced by digital processes, and the entire system becomes significantly more compact. Moreover, the signal processing function and trigger formation logic become more flexible compared to that in electronic pulses due to digitization. DDAQ systems have considerable advantages in some cases compared to conventional analog

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DAQ systems, especially when several complex channel signals are encountered [17–21].

Although the signal processing methods are significantly different for DDAQ compared to that in conventional DAQ, the trigger concept or logic remains the same. Generally, a trigger is formed from several signal channels that are necessary to define specific physical processes while excluding non-relevant processes as much as possible. The trigger is necessary to reduce the dead time of the DAQ system and save data storage space [22]. As the trigger logic must be defined by the user and may vary from one experiment to another, a flexible trigger system should be designed [5–8]. This can be realized in the DDAQ system using the rich logic operation capabilities provided by field programmable gate arrays (FPGAs) [23–26].

In a recent nuclear reaction experiment performed at the radioactive ion beam line at the Heavy Ion Research Facility in Lanzhou (HIRFL-RIBLL1) [27], we employed a DDAQ system based on hardware produced by XIA LLC [28] combined with a conventional DAQ system (VME). We provide a general description of this new combined DAQ system, which will be helpful for many other similar experiments. In Sect. 2, we describe the hardware of the DDAQ system. Section 3 describes the configuration of the flexible trigger system. Section 4 presents the application to experiments of different sizes. Section 5 presents the method for combining a conventional VME system with the newly developed DDAQ (XIA) system. Experimental test results are presented in Sect. 6, followed by a summary.

2 Basic Composition of a DDAQ system

2.1 Major components

The actual DDAQ system comprises five hardware components produced by XIA LLC [24]. One major component was the Pixie-16 6U Compact PCI/PXI crate. It hosts other plugin units, supplies local power, and transmits digital signals between the units. The second component was a PCI-8366/PXI-9369 crate controller, which served as the commander for the other modules and communicated with the computer. The computer sends messages to the DAQ system and obtains data from the memory of the modules through a CRATE controller. The third component was the Pixie-16 acquisition module. It converts the analog signal into digital data via a sampling method and extracts energy and time information from the input signal according to a predefined algebraic formula [24]. Various versions of Pixie-16 digitize the analog signal at sampling rates of 100, 250, or 500 MHz and store each sample in 12, 14, or 16 bits. The Pixie-16 acquisition module plays the role of a shaping amplifier, discriminator, ADC, and TDC in traditional DAQ (for example, VME) systems. The fourth component is the MicroZed-based Trigger IO (MZTIO) module containing the FPGA chip. The final component, the P16Trigger module, synchronizes the triggers, and clock signals across multiple crates [29].

The trigger system must combine the selected fast source signals to generate the main trigger signal that provokes the DAQ modules to extract and save data. A trigger source signal is generally a fast signal originating from a Pixie-16 acquisition module or MZTIO (based on commercial FPGA chip from Xilinx [30]) logic module. Several methods exist for forming and broadcasting the main trigger (see the sections below). In our design, the main trigger appears to be an external signal, called a “ module-validation trigger [28]. Thus, all Pixie-16 acquisition modules can be activated by the same main trigger.

2.2 Flexible configuration in FPGA

We designed and implemented a flexible framework for FPGA, as schematically shown in Fig. 1. The logic units in FPGA are presented as boxes in the figure, and the arrows indicate the flow direction of the digital signals. The trigger source signals originate from the input RJ45 connector on the left, pass through four optional layers of logic units, and exit to the right-side ports. The four logic-function layers were divided into two groups. One group contains the first two layers configured by “or”-gates and “and”-gates. The second group contains the last two layers configured by the downscale units and programmable (“or” / “and”) gates. The expanding widths of the arrows indicate an increasing number of signal channels. The maximum number of input or output ports was 48, which was constrained by RJ45 connectors. Each port can be programmed as inputs or outputs.

The logic units in the same layer are identical and independent of each other, and function according to their own parameter configurations. Moreover, all logic units are optional, meaning that each source signal may pass through the selected complex logic units or simply pass across all layers without any logic operation. This flexibility was implemented using a mask unit (upper part of Fig. 1) in front of a logic gate and a multiplexer [31] in front of a downscaled unit (see the second group in the figure). Both a mask and multiplexer were used to filter the input signals. The multiplexer has only a single output line, whereas a mask can send multiple outputs. Therefore, the “and”-gate or “or”-gate behind the mask unit can make logic operations on multiple input source signals, while the downscaler

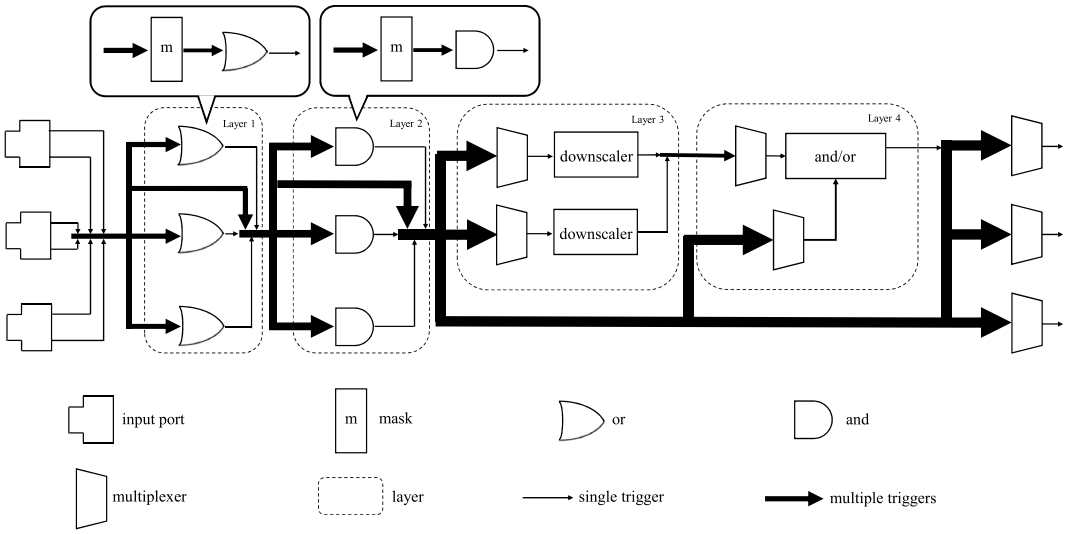

Fig. 1 Schematic of the FPGA configuration with four layers as contained in the dashed line squares. The arrows show the digital signal flows with thickness proportional to the involved channel numbers. The upper sub-figures show the logic gates with mask units and the lower panel gives the legend. See the text for more details

and programmable "and" / "or"-gates could manipulate one input signal from each multiplexer.

Based on the above configuration, the first group (layers 1 and 2) can perform almost all types of logic combinations for the input source signals. In practice, the first layer is dedicated to the "or" coincidence, while the second layer is dedicated to the "and" coincidence. A real example is presented in Sect. 2.3. In Fig. 1, only three gates are drawn. However, in an actual FPGA module, 16 gates are provided, which is sufficient for typical nuclear reaction experiments. Moreover, by applying the mask, one "or"-gate in the first layer may select any input source signal from the 48 input ports. Similarly, one "and"-gate in the second layer may select input signals from the 48 input ports and 16 outputs from "or"-gates, leading to 64 choices defined by the corresponding mask. This is also the reason that we see thicker arrows pointing to the "and"-gates compared with those pointing to the "or"-gates.

The second group served as the downscaling function. This is useful when some accompanying processes in an experiment are much more probable than other targeted physical processes. The recording of these high-rate accompanying processes must be suppressed to maintain a high DAQ efficiency for the processes of interest. For instance, if the accompanying rate is 50,000 Hz, a downscaling factor of 100 would reduce the rate of the output signals to 500 Hz, meaning one output for every 100 inputs. The fourth layer comprises programmable "or" / "and" gates. Each gate may receive two channels: one from the downscaler and the other directly from the second or earlier layer. Although we showed only one unit in the third and fourth layers (Fig. 1), four independent units are incorporated into each layer.

Table 1 Number of manipulable parameters in masks or multiplexers for each layer of the FPGA configuration

Layer	Unit	Parameter number
1	masks before "or"-gate	16×48
2	masks before "and"-gate	16×64
3	multiplexers in 3rd layer	4×1
4	multiplexers between 2nd and 4th layers	4×1
4	multiplexers between 3nd and 4th layers	4×1

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D0 = (A3 | A7) / 10
A2 = D0 | (((( A3 & A7 ) | A0 | A4 ) & A12 ) | B0 | B4)
B14 = D0 | (((( A3 & A7 ) | A0 | A4 ) & A12 ) | B0 | B4)
C21 = clock_5MHz
S0 = A3 | A7
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Fig. 2 An example of the FPGA configuration file written in script language

The above-described configuration in an FPGA is sufficiently flexible to meet the trigger-logic requirements of a general nuclear reaction experiment [5–8]. Trigger logic can simply be changed by editing the parameter values for masks and multiplexers with the help of a Xillybus Lite IP core [32]. The numbers of manipulable parameters in the masks or multiplexers for each layer are listed in Table 1. Since several tunable parameters might easily be confused in a practical setting, we developed software [33] that allows

reading a simple file written in script language and converting it into FPGA configuration parameters (see next section).

2.3 Configuration with the script language

An FPGA configuration file written in script language may comprise several lines of expression, such as those shown in Fig. 2. Each line expresses a logic calculation based on digital signals, which may include the logic "or" (|), logic "and" (&), fraction (/), etc. In the example (Fig. 2), the first line describes the logic "or" for the source inputs from ports A3 and A7, and the result is downscaled by a factor of 10 to form the output D0. We denote the 48 input ports as A0-A15, B0-B15, and C0-C15. The second line in Fig. 2 shows that the A2 outputs are equal to the complex logic result from signals D0, A0, A3, A4, A7, A12, B0, and B4. The third line is similar to the second line, but with outputs sent to port B14. Although the logic expression is complex and contains four layers, it can be converted into two layers expressed as "(A3 | A0 | A4 | B0 | B4)&(A7 | A0 | A4 | B0 | B4)&(A12 | B0 | B4)" in the software. This conversion is guaranteed by the distributive law [that is, A & (B | C) = (A & B) | (A & C)]. Obviously, the first layer will consider the expression in the parentheses and the second layer is related to the operator " &." This structural conversion is illustrated schematically in Fig. 3.

The fourth line in Fig. 2 is an additional function that generates a 5-MHz clock signal at port C21, and is used to match the timing between different DAQ systems, such as VME and XIA systems (more descriptions in Sect. 4). This is a periodic signal with logic "1" and "0", each occupying half of the period. The frequency is defined using the configuration file (5 MHz as an example). The fifth line defines a scaler called S0 that counts the frequency of the "or"-coincidence of A3 and A7. This function records one of the trigger rates used to monitor the online experiment and normalize the corresponding cross section in the data analysis.

The currently designed software can set up the FPGA in three steps: read the configuration file written in script language, convert its contents into FPGA configuration parameters, and write the parameters to the FPGA memory. It functions as a compiler that converts script expressions into configuration files. By using this software, the FPGA setup becomes easier to implement.

3 Application to small, medium, and large sized DAQs

The number of signal channels for a reaction experiment varies with the complexity of the real detection system, which is related to the physical processes to be measured. We define a small-sized DAQ system as one where the total number of signal channels can be accommodated in three data acquisition modules, that is, less than 48 channels. Medium size corresponds to a DAQ system using only one crate, that is, fewer than 11 data acquisition modules or 176 channels. A large-size DAQ system uses multiple crates. It is to be noted that these definitions can be changed by the DAQ users.

For all three types of DAQs, we used a central structure to manage data acquisition. The central structure divides the modules into central and local modules, as schematically shown in Fig. 4. The center module might be a pixie-16 acquisition module or an FPGA logic module, depending on the size of the DAQ, which generates the main trigger signal and controls data acquisition. Other pixie-16 acquisition modules are regarded as local. The central structure for all three size functions in five steps for one data recording cycle is depicted in Fig. 4: (1) the local pixie-16 acquisition module generates a fast trigger source signal from the electric analog signal; (2) the center module receives many trigger source signals; (3) the center module makes logical combinations of all received trigger source signals and generates the main trigger signal; (4) the center module sends the main trigger back to the local ones; (5) the local modules, according to the time match with the main trigger, proceed with the local signal and store the data.

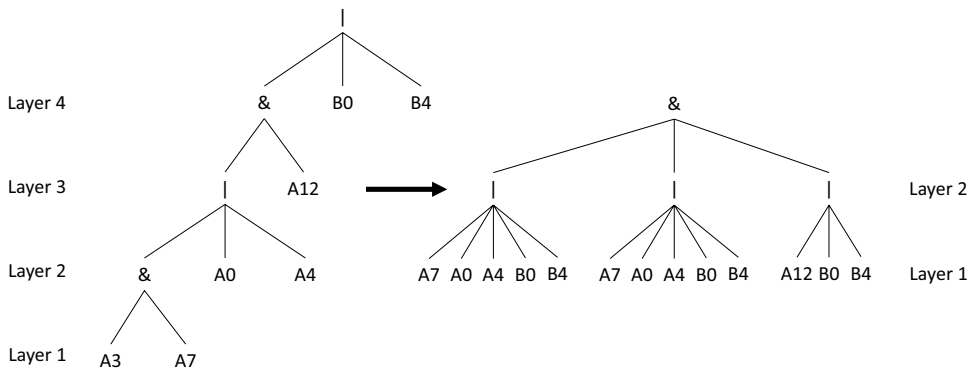

Fig. 3 Transformation of the logic expressions in parse tree structures [34] according to the distributive law

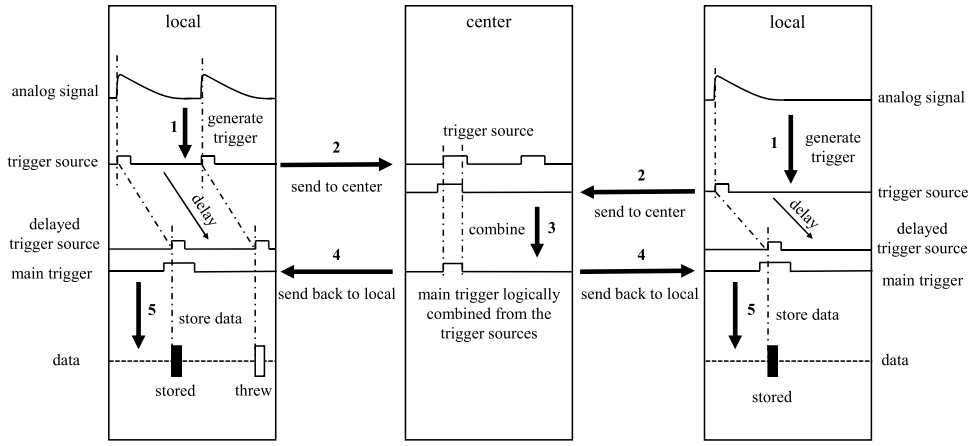

Fig. 4 Schematic of the signal flow in the DAQ central structure. The center module is presented in the middle and the local modules are on both sides

3.1 Small size DAQ

According to the design of the XIA system, a neighboring module can share the fast-trigger source signal without disturbing the other modules (not using the overall connection lines at the backplane of the crate). In the case of a small-sized DAQ, the three pixie-16 acquisition modules (48 channels in total) should be installed in neighboring slots, with the middle one serving as the center module and side ones as the local modules. In Step 2, the center module receives the trigger source signals from the two local modules via the dedicated neighboring connection. In Step 3, the middle (center) module combines the trigger source signals with the main trigger according to a preset built-in function. This function was designed using XIA, which allows the flexible setting of parameters for logical operations. The main trigger can then be broadcasted to all the local modules via common lines at the backplane of the crate.

3.2 Medium-size DAQ

In the case of a medium-sized DAQ, a logic FPGA module should be included as the center module. Since there may be up to ten trigger source signals from the local modules, they may disturb each other if common connection lines at the backplane of the crate are used. To avoid this problem, Category 6 (Cat 6) cables were used to connect the front panel of the local module and center module individually. In this manner, Step 2 can be realized safely. This method is limited by the number of RJ45 connectors on the front panel of the center logic module (12), and must be partially used for other purposes. An alternative approach, called "group connection," may be adopted for the RJ45 connectors. First, three neighboring local modules can be connected as a group via a dedicated neighboring connection line, and a grouped trigger source signal can be sent to the center according to built-in functions. This grouping is particularly reasonable when a single detector, such as a silicon strip or wire-plane detector, covers several 16-channel DAQ modules. As a result, the center module receives fewer source signals from the front panel in Step 2, and then broadcasts the main trigger signal to each local module via the common lines at the backplane of the crate in Step 4. Evidently, this method can only be applied to DAQs with a single crate.

3.3 Large-size DAQ

In the case of a large DAQ, several crates must be controlled by the same center module. The grouped trigger sources described above can still be used in Step 2. However, the broadcast of the main trigger in Step 4 cannot be realized via the backplane of a single crate. Next, Step 4 is divided into two substeps. The first substep involves sending the main trigger through a Cat 6 cable to a relayed module in each crate. In the second step, the relayed module broadcasts the main trigger through the backplane of its host crate. Although this solution is significantly complex and limited by the number of RJ45 connectors, it maintains synchronization between the crates and modules, and simplifies the parameter settings in all modules. For an even more complex DAQ system, it is necessary to use multiple logic FPGA modules with more complicated connection configurations and parameter settings.

3.4 Signal timing matching

As described in the Introduction, experimental data must be recorded and analyzed according to physical events. In other words, the data in different signal channels should coincide such that they correspond to the same experimental event. However, signals in different channels may experience

different processing times during their detection, pre-amplification, analog signal transmission, digitization, and logic operation. Therefore, a trigger system should be set considering these differences. Here, we assume that the timing differences for the analog signal have already been addressed by setting the offsets based on the measurements. Then, we consider only the processes in DAQ, which involves three steps are as follows. The first step is to match the trigger source signal within one module or from a neighboring module. Some jitters exist among the signals as a result of fluctuations in the detection and electronics systems, noise signals, signal-shape uncertainties, and a small diversity of hardware products. Hence, the width of the trigger source signal is set to 400 ns to cover the jitter. Additionally, source signals from modules with a 250-MHz sampling rate should be delayed for approximately 60 ns to be consistent with modules having sample rates of 100 MHz or 500 MHz. The second step is to match the trigger-source signals from different local modules. This was performed in the central logic module by setting the offsets for each received source signal. Occasionally, this step can be ignored as long as the first step already provides sufficient matching. The third step matched the data signals in the local modules with the main trigger signal sent from the central module. The main trigger lags behind the local source (or data) signals by approximately 200 ns, which can be compensated for by applying a delay to the local signals (see Fig. 4). Considering the jitter of the local signals, the width of the main trigger signal is generally set to 500 ns or longer to ensure a good overlap with all good data signals in the local modules. Thus, to achieve a good overlap of all local data signals with the wide main trigger signal, the delay time of the local data signals should be increased to 450 ns (200 ns + 250 ns).

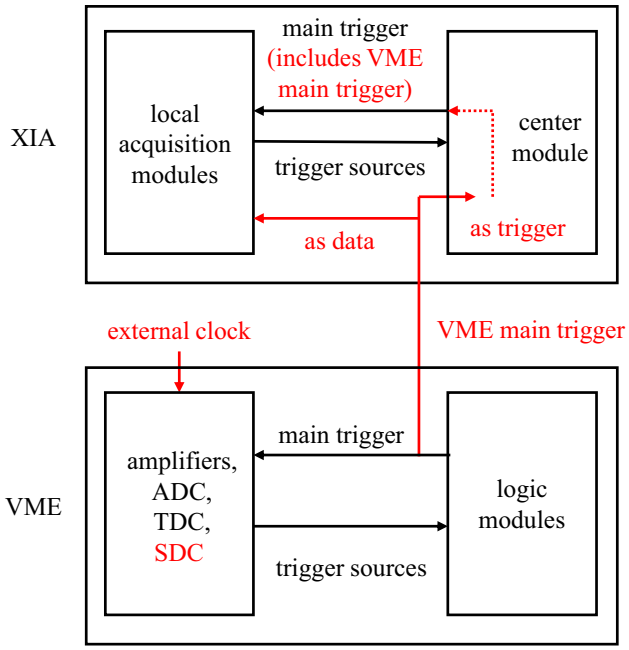

Fig. 5 Schematic of the combination between the XIA and the VME systems

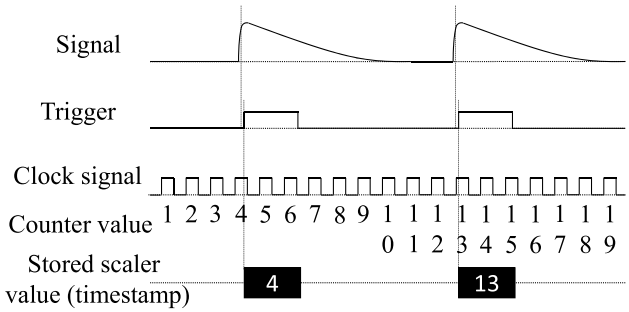

Fig. 6 The concept for recording the timestamps by the V830 module in a VME system

4 Combination of the DDAQ system with the conventional DAQ system

Although there are advantages to using DDAQ systems, as stated in the Introduction, the conventional DAQ (for example, VME) system is still useful because of its availability with a large number of existing modules and crates. Therefore, in the case of a shortage of XIA modules, XIA and VME systems can be used in combination [35, 36]. However, for this type of mixed system, event alignment (matching) between the two systems is essential. In a conventional DAQ system, data are stored according to the number of physical events (triggers), with each event containing information (energy, time, etc.) from all the channels. On the other hand, the XIA system successively records the signal information from each channel with the timestamps. Thus, a physical event corresponds to signal information distributed in several channel data packages that are correlated only by their timestamps. Additionally, owing to the fast signal processing capability of the XIA system, it can be used to record high-rate signals, such as those from detectors at forward angles. Moreover, the VME system may be applied to low-rate signals, such as those from large-angle detectors. Since each system has its own trigger setting and operation, a high number of events can be recorded by the XIA system in comparison to those recorded by the VME system. Therefore, it is essential to determine the correspondence between the VME event number and XIA timestamp.

This problem can be resolved by recording timestamps in the VME system and aligning them in both systems [35, 36]. In the XIA system, a timestamp represents the duration

from the start of the data-recording run (data file). Typically, the timing is represented by clock numbers. For example, in an XIA system, the clock frequency is the same as the sampling rate, for example 100 MHz, or a period of 10 ns. Thus, a timestamp of 200 indicates 2 μs from the run-start time.

The following modifications were incorporated to the DAQ system to set and match the timestamps, as schematically shown in Fig. 5. First, we adopted a V830 scaler module (marked as SDC in Fig. 5) in the latching scalar mode of the VME system [37]. It records timestamps when the input signal is a periodic clock signal, as shown in Fig. 6. For example, two VME triggers may randomly coincide with the 4th and 13th clock cycles. Then, the V830 scaler records numbers 4 and 13 into the corresponding event data, stamping the VME events at 400 ns and 1300 ns when the clock frequency is 10 MHz. The clock signals are usually generated from the XIA-FPGA chip. Therefore, the clock frequency should be selected appropriately. A significantly high frequency may cause memory overflow and bit flipping in the V830 module, whereas a low frequency deteriorates the time resolution in the subsequent matching procedure. A clock rate of 5 MHz was used in the previous experiment (see the section below).

To align the timestamps in both the VME and XIA systems, we set the VME main trigger to the XIA system to be included in the XIA trigger series and recorded it as one-channel data, as depicted in Fig. 5. This enables comparing the timestamps of the XIA and VME systems for common trigger signals. Since the processing time for a common trigger signal in either system is constant during the entire data acquisition run, the difference between the timestamps of the two systems should also be constant. This conclusion remains valid even if the run (file) starting times in both systems differ slightly owing to the manual control method. Evidently, only the time offset should be determined to match the two systems. This offset can easily be fixed by scanning the time differences in both systems for all common trigger signals at each offset setting, as shown in Fig. 7. As a matter of fact, the common trigger signals initiated by the VME system are randomly distributed in time. If the offset is incorrect, as indicated by the two upper lines in Fig. 7, the ratio of the matched trigger number to the total number of triggers must be small. By contrast, the matched rate can be closed to 1.0 when the correct offset is applied (see the lower panel of Fig. 7). To find the correct offset, we can simply step the offset in an estimated time range and check the matching rate. The match number is increased when common trigger signals appear in both the VME and XIA systems within a small time window, as indicated by the pair of diagonal dashed lines in the upper panel of Fig. 7. The width of this time window must be smaller than the average time interval between adjacent common trigger signals. This interval is approximately 10 ms in the most recent experiments. After determining the highest match rate (over 95% for our experiment), the offset can still be fine-tuned to obtain the exact timing overlaps of the corresponding trigger signals.

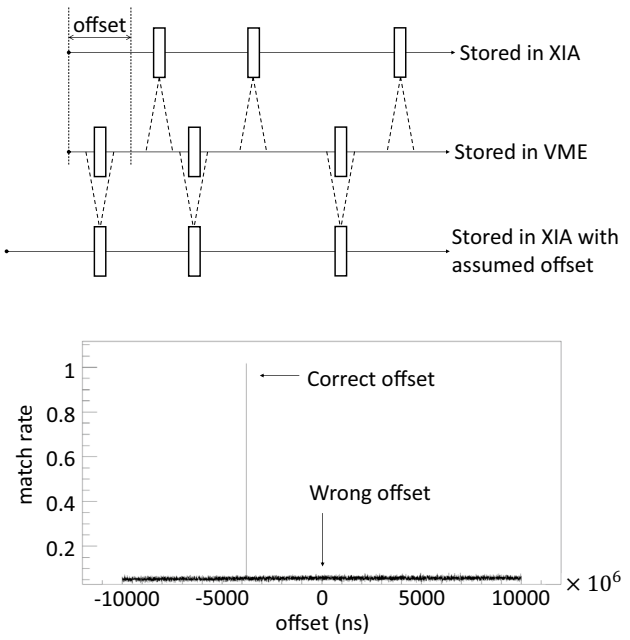

Fig. 7 The algorithm (upper panel) and performance (lower panel) for matching the timestamps in both VME and XIA systems

5 Experimental test results

The combined DAQ system was applied in a nuclear reaction experiment at the radioactive ion beamline of HIRFL-RIBLL1 [27]. Several beams, such as ^{14}C and ^{16}C, were used with beam intensities of approximately 5×10^4 pps. In this experiment, multiple layers of silicon strip detectors were mounted at 0° to detect decay fragments at forward angles. An annular telescope comprising a layer of silicon strip detectors and an array of CsI(Tl) scintillators was installed to cover larger scattering angles. The essential part of the trigger logic is to record an event with multiple decay fragments hitting the silicon strips on the zero-degree detectors, or any particle hitting the large-angle annular telescope. Since the number of single-hit events on the zero-degree detector was large, these events were downscaled by the DAQ corresponding to the incident of the direct beam to reduce the total trigger rate. Therefore, each recorded event must belong to one of three types of events: 1) multiple hits in the zero-degree detector, 2) a single hit in the zero-degree detector but subjected to sampling, or 3) any hit in the annular

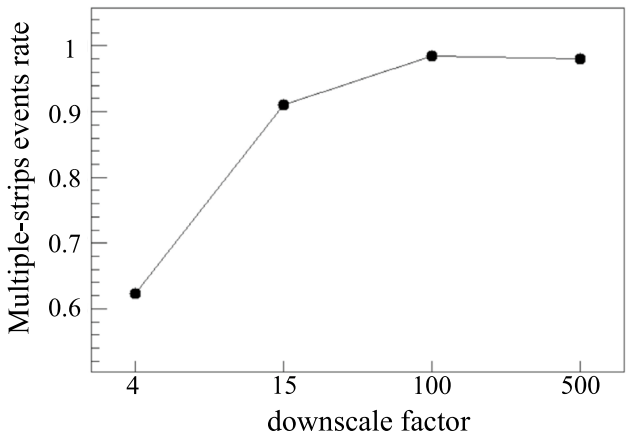

Fig. 8 The multiple-strip event rate (in the zero-degree detector) normalized to the total event rate (filled circles), as a function of the downscaling factor

detector. The counting rates for these three types of events were approximately 2×10^4, 3.5×10^4 (before downscaling) and below 100, respectively. Due to the fast capacity of the XIA system, type-1 and type-2 events were recorded, whereas type-3 events were recorded by the VME system and partially by the XIA system for cross DAQ verification (see next paragraph). Owing to the limited capacity of the DAQ system, reducing the number of forward-angle single-hit events is important for maintaining high efficiency (high live-time rate) for multiple-hit events. Figure 8 shows the ratio of multiple-hit events to the total recorded events, which increases with an increasing downscale factor for single-hit events. We note that the trigger rate in the VME system associated with large-angle detection by annular telescopes is independent of the XIA system, and thus, was not affected by downscaling in the XIA system. During the experiment, we maintained a live-time rate higher than 90% for the DDAQ system (after downscaling), whereas this rate was always ~ 100% for the VME system owing to its very low trigger rate.

As shown above, some data detected by the annular telescope were recorded by both the VME and XIA systems, which can be used to verify the correctness of the timestamp matching between the two systems. Figure 9 shows a particle identification (PID) spectrum using the energy loss ΔE detected by the first layer of the annular telescope (Si strip) and recorded by the VME system versus the remaining energy E detected by the second layer (CsI(Tl)) and recorded by the XIA system. The clear PID curves for the H and He isotopes demonstrate perfect matching of the two DAQ systems.

6 Summary

DDAQ based on hardware products from XIA LLC was applied to a complex nuclear reaction experiment. A flexible FPGA logic configuration was implemented for trigger handling. Software was developed that allows the conversion of the simplified logic definition in script language into the system's internal parameters. Moreover, the central structure (central and local modules) of DDAQ provides convenient solutions for small, medium, and large experiments. A practical method was established to combine the DDAQ (XIA) and conventional DAQ (VME) systems, which is particularly useful for the current transition from conventional DAQ to DDAQ. The combined system was successfully applied to a complex nuclear reaction

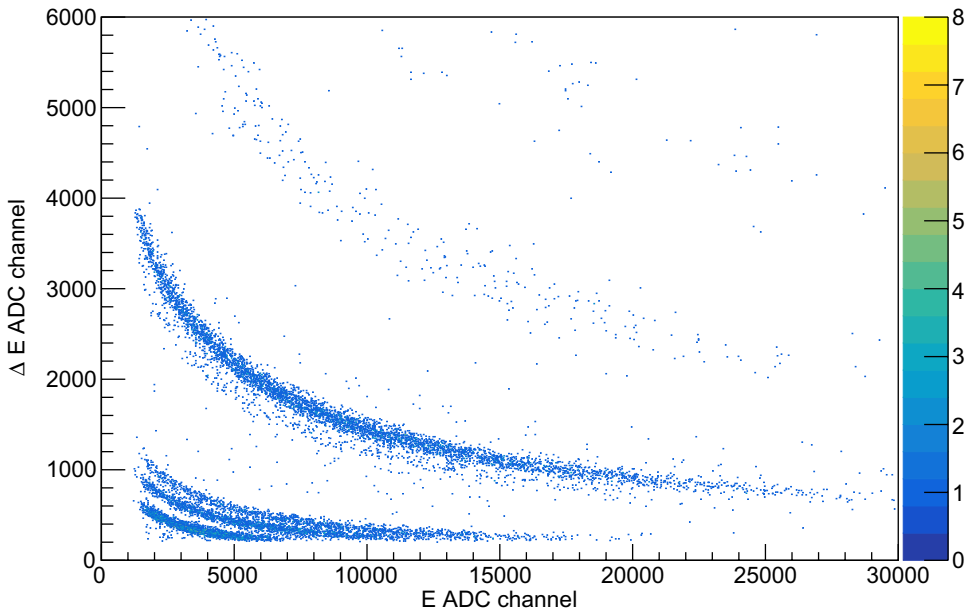

Fig. 9 (Color online) The $\Delta E - E$ PID spectrum detected by the annular telescope, with ΔE recorded by the VME system and E by the XIA system

experiment using HIRFL-RIBLL1. The present work will be of interest to experimentalists adopting DDAQ in the coming years.

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Author Contributions All authors contributed to the study conception and design and also the data collection and analysis. The present DDAQ application codes were realized by W-LP. The first draft of the manuscript was written by W-LP and all authors made revision on previous versions of the manuscript. All authors read and approved the final manuscript.

Data availibility The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.14278 and https://www.doi.org/10.57760/sciencedb.14278.

Declarations

Conflict of interest The authors declare that they have no competing interests.

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